WE CLAIM:

1. A method of pre-emphasizing an output signal in response to receiving an input signal undergoing a voltage transition, said input signal being at an input voltage level after said transition, said method comprising:

outputting said output signal at a first voltage level for a first period of time, said first voltage level greater in magnitude than said input voltage level, said first period of time less than a baud period; and

decreasing the magnitude of said output signal via a series of voltage levels, each voltage level of said series remaining substantially constant for a period of time less than a baud period, each voltage level of said series smaller in magnitude than a prior voltage level and greater in magnitude than said input voltage level.

2. The method of claim 1 wherein said decreasing the magnitude of said output signal comprises decreasing the magnitude to a second voltage level for a second period of time, said second voltage level smaller in magnitude than said first voltage level and greater in magnitude than said input voltage level, said second period of time less than a baud period.

3. The method of claim 2 further comprising decreasing the magnitude of said output signal to a third voltage level for a third period of time after said decreasing to said second voltage level, said third voltage level smaller in magnitude than said second voltage level and greater in

4. The method of claim 3 further comprising decreasing the magnitude of said output signal to said input voltage level after said decreasing to said third voltage level.

5. The method of claim 1 further comprising decreasing the magnitude of said output signal to said input voltage level after said decreasing the magnitude of said output signal via a series of voltage levels.

6. The method of claim 1 wherein the sum of all said time periods equals a baud period.

7. The method of claim 1 wherein the sum of all said time periods is greater than a baud period.

8. The method of claim 1 wherein:

said input voltage level is a positive voltage representing a logical 1 value; and

said first voltage level is a more positive voltage than said input voltage level.

9. The method of claim 1 wherein:

said input voltage level represents a logical 0 value; and

said first voltage level is a voltage less than or more negative than said input voltage level.

10. A method of pre-emphasizing an output signal in response to receiving an input signal undergoing a voltage transition, said input signal being at an input voltage level after said transition, said method comprising:

outputting said output signal at a first voltage level for a first period of time, said first voltage level greater in magnitude than said input voltage level, said first period of time less than a baud period; and

sinking a first amount of current after said first period of time to reduce said first voltage level to a second voltage level, said second voltage level smaller in magnitude than said first voltage level and greater in magnitude than said input voltage level; and

sinking a second amount of current after a second period of time concurrently with said first sinking to reduce said second voltage level to a third voltage level, said third voltage level smaller in magnitude than said second voltage level and greater in magnitude than said input voltage level, said second period of time less than a baud period.

11. The method of claim 10 wherein said sinking a first amount of current comprises activating a first current source after a first delay of said input signal.

12. The method of claim 10 wherein said sinking a second amount of current comprises activating a second current source after a second delay of said input signal, said second delay greater than said first delay, said first and second current sources active concurrently after said second delay.

13. The method of claim 10 further comprising sinking a third amount of current after a third period of time concurrently with said first and second sinking to reduce said third voltage level to said input voltage level.

14. A method of pre-emphasizing an output signal in response to receiving an input signal undergoing a voltage transition, said input signal being at an input voltage amplitude after said transition, said method comprising:

generating said output signal at a first voltage amplitude for a first period of time, said first voltage amplitude greater than said input voltage amplitude, said first period of time less than a baud period;

reducing said output signal voltage amplitude to a voltage level between said first voltage amplitude and said input voltage amplitude for a period of time less than a baud period;

repeating said reducing at least once; and

reducing said output signal voltage amplitude to about said input voltage amplitude after at least one baud period.

15. A circuit operative to pre-emphasize an output signal in response to receiving an input signal undergoing a voltage transition, said circuit comprising:

a input node operative to receive said input signal;

an output node;

a delay line coupled to said input node, said delay line comprising a plurality of output nodes each

operative to output a signal having a different delay with respect to said input signal;

a signal driver coupled to said input node and to said ouput node, said driver operative to output a signal at any one of a plurality of degrees of amplification with respect to said input signal;

a plurality of current sources coupled to said signal driver, each of said current sources operative to draw current from said signal driver and each being individually enabled by a separate enable signal, enablement of each said current source reducing the amplification of said driver output signal; and

control logic coupled to said delay line output nodes and respectively coupled to each of said current sources, said control logic operative to generate said separate enable signals either individually or concurrently in response to inputs received from said delay line output nodes, said control logic generating no enable signals for at least a portion of a baud period and generating at least one enable signal for least another portion of said baud period.

16. The circuit of claim 15 wherein said delay line comprises a plurality of serially-connected latches, each latch output coupled to a respective delay line output node.

17. The circuit of claim 15 wherein said delay line and control logic comprise:

a plurality of serially-connected latches, each latch output coupled to a respective delay line output node, each latch operative to receive a control signal;

a ring oscillator operative to generate an output signal, said oscillator having the same number of delay stages as the number of said serially-connected latches;

a phase detector operative to receive a clock signal and said ring oscillator output signal and operative to output a signal indicating a phase difference; and

a charge pump/loop filter operative to receive said phase detector output signal and to output said control signal.

18. The circuit of claim 15 wherein said signal driver comprises current mode logic (CML) circuitry.

19. The circuit of claim 15 wherein said signal driver comprises low voltage differential signaling (LVDS) circuitry.

20. A transmitter circuit comprising said circuit of claim 15.

21. A transceiver circuit comprising said circuit of claim 15.

22. An integrated circuit chip comprising said circuit of claim 15.

23. A programmable logic device comprising said circuit of claim 15.

24. A printed circuit board comprising said circuit of claim 15 mounted on said printed circuit board.

25. The printed circuit board of claim 24 further comprising a memory mounted on said printed circuit board.

26. The printed circuit board of claim 24 further comprising processing circuitry mounted on said printed circuit board.

27. A digital processing system comprising:

a processor;

a memory coupled to said processor; and

said circuit of claim 15 coupled to at least one of said processor and said memory.

28. A digital processing system comprising:

a processor; and

a memory coupled to said processor, wherein at least one of said processor and said memory comprises said circuit of claim 15.

29. A circuit operative to pre-emphasize an output signal in response to receiving an input signal undergoing a voltage transition, said circuit comprising:

a input node operative to receive said input signal;

an output node;

a delay line coupled to said input node, said delay line comprising a plurality of output nodes each

operative to output a signal having a different delay with respect to said input signal;

a signal driver coupled to said input node and to said ouput node, said driver operative to output a signal at any one of a plurality of degrees of amplification with respect to said input signal;

a plurality of current sources coupled to said signal driver, each of said current sources operative to draw current from said signal driver and each being individually enabled by a separate enable signal, enablement of each said current source reducing the amplification of said driver output signal; and

control logic coupled to said delay line output nodes and respectively coupled to each of said current sources, said control logic operative to generate said separate enable signals either individually or concurrently in response to inputs received from said delay line output nodes.

30. Apparatus for pre-emphasizing an output signal in response to receiving an input signal undergoing a voltage transition, said input signal being at an input voltage level after said transition, said apparatus comprising:

means for outputting said output signal at a first voltage level for a first period of time, said first voltage level greater in magnitude than said input voltage level, said first period of time less than a baud period; and

means for decreasing the magnitude of said output signal to a second voltage level for a second period of time, said second voltage level smaller in magnitude than said first

voltage level and greater in magnitude than said input voltage level, said second period of time less than a baud period.

31. Apparatus for pre-emphasizing an output signal in response to receiving an input signal undergoing a voltage transition, said input signal being at an input voltage amplitude after said transition, said apparatus comprising:

means for generating said output signal at a first voltage amplitude for a first period of time, said first voltage amplitude greater than said input voltage amplitude, said first period of time less than a baud period;

means for reducing said output signal voltage amplitude to a voltage level between said first voltage amplitude and said input voltage amplitude for a period of time less than a baud period;

means for repeating said reducing at least once; and

means for reducing said output signal voltage amplitude to about said input voltage amplitude after at least one baud period.